

CmpE Internship Summer 2018

Design Doc Template

Dial Controlled Flashlight

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| --- | --- | --- |
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Table of Contents

[Objective](#_f3ut0x3v9lxf) 2

[Background](#_52hjxc9p7ctt) 2

[Overview](#_yy2djj5i8omd) 3

[Detailed Design](#_avw48lx4cmyr) 4

[Caveats](#_op45shsa5n8y) 5

[Testing Plan](#_eejuf5av24ql) 5

[Unit testing scheme](#_h5m3fobrdlly) 5

[Integration Testing](#_fubwzje1thtf) 5

[Demonstration Project](#_6z1lojsl95dl) 5

# Objective

A few sentences, describing the key system objectives.

In this project I aim to create a system of LEDs that are controlled/activated depending on the current position of a rotary encoder. As this rotary encoder is turned, the LEDs turn on/off as the encoded signal changes.

# Background

Information that others would need to know to understand this design document. (related documents, previous versions etc.)

Input Device: Rotary Encoder - <https://reference.digilentinc.com/reference/pmod/pmodenc/reference-manual>

Output Device: Eight High Brightness LEDs - <https://reference.digilentinc.com/reference/pmod/pmod8ld/reference-manual>

# Overview

Based on my current understanding, an overview of this task includes creating the state machine for our PMOD devices, followed by writing the code for the MIPS processor to interface with that state machine.

The rotary encoder essentially provides 4 digital input signals. The two represent the value of the on-board switch as well as an integral push button/slide switch in the shaft, and can be used as enable signals. The following two signals represent the outputs of the encoded signal. Looking at the timing of the rising edges of these signals we can deduce the direction the dial is being turned.

The eight high-brightness LEDs are very straight forward. The pins controlling the LEDs are active high, so to activate an LED a high voltage must be applied.

# 

# Detailed Design

Detailed description of what you are designing and how.

# 

# Caveats

* Debouncing the signals provided by the rotary encoder

# Testing Plan

### Unit testing scheme

* Simulate bounced inputs in Verilog to ensure debouncing is secured.
* Unit test each major submodule as they are developed.
* Simulate a rotating input and monitor how my state machine’s outputs respond.

### Integration Testing

Describe how you will go about doing integration testing (i.e. testing on the SJTwo board).

* Once all the submodules are fully tested and assured to be functioning, the mapping of them in the top modules can also be tested.

### Demonstration Project

N/A